CLAIMS

We claim:

1. A sense amplifier for a memory array providing increased reliability in sensing small voltage differences, comprising:

two cross coupled inverters forming a latch;

supply coupling means for selectively connecting the latch to a supply source; and

bit line coupling means for selectively connecting inputs of each inverter to complimentary bit lines from the memory array; and

delaying means for delaying the disconnection of the bit lines from the sense amplifier.

2. The sense amplifier of claim 1, further comprising compensating means for correcting an offset between the inverters of the latch and the supply coupling means.

3. The sense amplifier of claim 1 wherein the supply coupling means comprise an NMOS transistor.

4. The sense amplifier of claim 1 wherein the bit line coupling means comprise a PMOS transistor connected in series between each complimentary bit line and the latch.

5. The sense amplifier of claim 2 wherein the compensating means comprise a pair of NMOS transistors connected between the latch and the common supply terminal.

6. The sense amplifier of claim 2 wherein the supply coupling means is controlled by a strobe signal.

7. An The sense amplifier of claim 6 wherein the strobe signal to disable the supply coupling means is delayed by the delaying means.

8. The sense amplifier of claim 1 wherein the delaying means comprises a plurality of inverters connected in series.

9. A method for improving a latch-type sense amplifier for a memory array in order to increase reliability in sensing small voltage differences, comprising the steps of:

cross coupling two inverters to form a latch;

selectively coupling the latch to a supply source;

selectively coupling the inputs of each inverter to complimentary bit lines from the memory array; and

delaying the disconnection of the bit lines from the sense amplifier until a predetermined duration after the enabling of the sense amplifier latch.

10. The method for improving a latch-type sense amplifier of claim 9, further comprising the step of correcting the offset mismatch between the inverters of the latch and the supply coupling means.

11. The method for improving a latch-type sense amplifier of claim 10 wherein the offset correction is performed by providing degenerative feedback in the supply terminal path of the latch transistors that operate in the saturation mode.

12. The method for improving a latch-type sense amplifier of claim 9 wherein the disconnection of the bit lines is delayed by utilizing a delayed version of a sense amplifier enable signal to disconnect the bit lines.

13. An amplifier for a memory array, comprising:

a latch circuit;

a switch circuit configured to selectively connect inputs of the latch circuit to complementary bit lines from the memory array; and

a delay circuit coupled to the switch circuit and configured to delay a disconnection of the bit lines from the latch circuit.

14. The amplifier of claim 13 wherein the latch comprises first and second inverters cross-coupled together.

15. The amplifier of claim 14 wherein the inverters are formed of CMOS transistors.

16. The amplifier of claim 14, further comprising a compensation circuit coupled to the latch and configured to correct for an offset between the inverters of the latch and a supply coupling circuit that selectively connects the latch to a voltage supply source.

17. The amplifier of claim 13 wherein the delay circuit is configured to generate a delayed enable signal in response to a sense amplifier enable signal.

18. An amplifier circuit for a memory array, comprising:

a first PMOS transistor having a first terminal coupled to a voltage source, a second terminal coupled to a first node, and a control gate coupled to a second node;

a second PMOS transistor having a first terminal coupled to the voltage supply source, a second terminal coupled to the second node, and a control gate coupled to the first node;

a first NMOS transistor having a first terminal coupled to the first node, a control gate coupled to the second node, and a second terminal coupled to a third node;

a second NMOS transistor having a first terminal coupled to the second node, a control gate coupled to the first node, and a second terminal coupled to a fourth node;

a third NMOS transistor having a first terminal coupled to the third node, a control gate coupled to the second node, and a second terminal;

a fourth NMOS transistor having a first terminal coupled to the fourth node, a control gate coupled to the first node, and a second terminal coupled to the second terminal of the third NMOS transistor;

a fifth NMOS transistor having a first terminal coupled to the second terminals of the third and fourth NMOS transistors, a second terminal coupled to a voltage reference, and a control gate coupled to a sense amplifier enable signal source;

a third PMOS transistor having a first terminal coupled to the first node, a second terminal configured to be coupled to a first bit line of the memory array, and a control gate coupled to a delayed sense amplifier enable signal source; and

a fourth PMOS transistor having a first terminal configured to be coupled to a second bit line of the memory array, a second terminal coupled to the second node, and a control gate coupled to a delayed sense amplifier enable signal source.

19. The amplifier of claim 18 wherein the delayed sense amplifier enable signal source comprises an input coupled to the sense amplifier enable signal source and an output, and further comprising first and second series-coupled inverters, the first inverter having an input coupled to the input of the delayed sense amplifier enable signal source and an output coupled to the output of the delayed sense amplifier enable signal source.

20. The amplifier of claim 18 wherein the first PMOS transistor and first NMOS transistor form a first inverter circuit, the second PMOS transistor and second NMOS transistor form a second inverter circuit, the first and second inverter circuits comprising a latch, and further wherein the third and fourth NMOS transistors form a compensating circuit configured to correct a voltage offset between the first and second inverter circuits of the latch and the fifth NMOS transistor.

21. A method for sensing voltage differences in a memory array, comprising the steps of:

enabling a latch circuit;

selectively coupling inputs of the latch circuit to complementary bit lines of the memory array; and

disconnecting the latch circuit from the complementary bit lines after a predetermined delay from the step of enabling of the latch circuit.

22. The method of claim 21 wherein enabling the latch circuit comprises selectively coupling the latch circuit to a supply source.

23. The method of claim 22, further comprising the step of generating a delayed disconnect signal that initiates disconnection of the latch circuit from the complementary bit lines.

24. The method of claim 21, further comprising the step of correcting a voltage offset mismatch between inverters of the latch circuit and a circuit for enabling the latch circuit.

25. The method of claim 24 wherein the step of correcting the voltage offset mismatch comprises providing degenerative feedback in a supply terminal path of the inverter transistors that operate in a saturation mode.